CLAIMS

What is claimed is:

1 1.   A data transfer block for use in an integrated circuit (IC) to interface an on-

2 chip subsystem to an on-chip bus, the data transfer block comprising:

3   a first and a second outbound queue to facilitate selective staging of a first

4 and a second plurality of outbound bus transactions for the on-chip subsystem, at

5 the choosing of the on-chip subsystem, each of said outbound bus transactions

6 including a bus arbitration priority; and

7   a first state machine coupled to the first and second outbound queues to

8 service the first and second outbound queues, serially requesting for access to the

9 on-chip bus for the staged outbound bus transactions, according the first queue a

10 first outbound priority and the second queue a second outbound priority, where

11 access to the on-chip bus is granted to requesting bus transactions based at least in

12 part on the included bus arbitration priorities of the contending bus transactions.

1 2.   The data transfer block of claim 1, wherein said data transfer block further

2 comprises a configuration register coupled to said first state machine to store said

3 first and second priorities to be accorded to said first and second outbound queues

4 by said first state machine in servicing said first and second outbound queues.

1   3.   The data transfer block of claim 1, wherein

2   the data transfer block further comprises a third outbound queue, which in

3   conjunction with said first and second outbound queues, facilitates selective staging

4   of a third and said first and second plurality of outbound bus transactions for the on-

5   chip subsystem, at the choosing of the on-chip subsystem, with each of the

6   outbound bus transactions including a bus arbitration priority; and

7   said first state machine is also coupled to said third outbound queue, and

8   service said third outbound queue, along with said first and second outbound

9   queues, serially requesting for access to the on-chip bus for the staged outbound

10   bus transactions, according the third queue a third outbound priority complementing

11   said first and second outbound priorities accorded to the first and second outbound

12   queues, where access to the on-chip bus is granted to requesting bus transactions

13   based at least in part on the included bus arbitration priorities of the contending bus

14   transactions.

1   4.   The data transfer block of claim 1, wherein the data transfer block further

2   comprises

3   a first and a second inbound queue to facilitate selective staging of a first and

4   a second plurality of inbound bus transactions for the on-chip subsystem, at the

5   choosing of originating subsystems of the inbound bus transactions, each of the

6   inbound bus transaction including a bus arbitration priority and being granted access

7   to the on-chip bus based at least in part on the included bus arbitration priority; and

8   a second state machine coupled to the first and second inbound queues to

9   service the first and second inbound queues, serially bringing the staged inbound

10   bus transactions to the attention of the on-chip subsystem, according the first

11   inbound queue a first inbound priority and the second inbound queue a second

12   inbound priority.

1   5.   The data transfer block of claim 4, wherein said data transfer block further

2   comprises a configuration register coupled to said second state machine to store

3   said first and second inbound priorities to be accorded to said first and second

4   inbound queues by said second state machine in servicing said first and second

5   inbound queues.

1   6.   The data transfer block of claim 1, wherein

2   the data transfer block further comprises a third inbound queue, which in

3   conjunction with said first and second inbound queues, facilitates selective staging of

4   a third and said first and second plurality of inbound bus transactions for the on-chip

5   subsystem, at the choosing of originating subsystems of the inbound bus

6   transactions, with each of the inbound bus transactions including a bus arbitration

7   priority, and granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   said second state machine is also coupled to said third inbound queue, and

10   service said third inbound queue, along with said first and second inbound queues,

11   serially bringing the staged inbound bus transactions to the attention of the on-chip

12   subsystem, according the third queue a third inbound priority complementing said

13   first and second inbound priorities accorded to the first and second inbound queues.

1   7.   A data transfer block for use in an integrated circuit (IC) to interface an on-

2   chip subsystem to an on-chip bus, the data transfer block comprising:

3   a first and a second inbound queue to facilitate selective staging of a first and

4   a second plurality of inbound bus transactions for the on-chip subsystem, at the

5   choosing of originating subsystems of the inbound bus transactions, each of the

6   inbound bus transaction including a bus arbitration priority and being granted access

7   to the on-chip bus based at least in part on the included bus arbitration priority; and

8   a state machine coupled to the first and second inbound queues to service

9   the first and second inbound queues, serially bringing the staged inbound bus

10   transactions to the attention of the on-chip subsystem, according the first inbound

11   queue a first inbound priority and the second inbound queue a second inbound

12   priority.

1   8.   The data transfer block of claim 7, wherein said data transfer block further

2   comprises a configuration register coupled to said state machine to store said first

3   and second inbound priorities to be accorded to said first and second inbound

4   queues by said state machine in servicing said first and second inbound queues.

1   9.   The data transfer block of claim 7, wherein

2   the data transfer block further comprises a third inbound queue, which in

3   conjunction with said first and second inbound queues, facilitates selective staging of

4   a third and said first and second plurality of inbound bus transactions for the on-chip

5   subsystem, at the choosing of originating subsystems of the inbound bus

6   transactions, with each of the inbound bus transactions including a bus arbitration

7   priority, and granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   said state machine is also coupled to said third inbound queue, and service

10   said third inbound queue, along with said first and second inbound queues, serially

11   bringing the staged inbound bus transactions to the attention of the on-chip

12   subsystem, according the third queue a third inbound priority complementing said

13   first and second inbound priorities accorded to the first and second inbound queues.

1   10.   A subsystem of an integrated circuit, the subsystem comprising:

2   core subsystem logic; and

3   a data transfer unit to couple the core subsystem logic to an on-chip bus of

4   the integrated circuit, the data transfer unit including

5   a first and a second outbound queue to facilitate selective staging of a first

6   and a second plurality of outbound bus transactions for the core

7   subsystem logic, at the choosing of the core subsystem logic, each of

8   said outbound bus transactions including a bus arbitration priority; and

9   a first state machine coupled to the first and second outbound queues to

10   service the first and second outbound queues, serially requesting for

11   access to the on-chip bus for the staged outbound bus transactions,

12   according the first queue a first outbound priority and the second

13   queue a second outbound priority, where access to the on-chip bus is

14   granted to requesting bus transactions based at least in part on the

15   included bus arbitration priorities of the contending bus transactions.

1   11.   The subsystem of claim 10, wherein said data transfer unit further comprises

2   a configuration register coupled to said first state machine to store said first and

3   second priorities to be accorded to said first and second outbound queues by said

4   first state machine in servicing said first and second outbound queues.

1   12.   The subsystem of claim 10, wherein

2   the data transfer unit further comprises a third outbound queue, which in

3   conjunction with said first and second outbound queues, facilitates selective staging

4   of a third and said first and second plurality of outbound bus transactions for the core

5   subsystem logic, at the choosing of the core subsystem logic, with each of the

6   outbound bus transactions including a bus arbitration priority; and

7   said first state machine is also coupled to said third outbound queue, and

8   service said third outbound queue, along with said first and second outbound

9   queues, serially requesting for access to the on-chip bus for the staged outbound

10 bus transactions, according the third queue a third outbound priority complementing

11 said first and second outbound priorities accorded to the first and second outbound

12 queues, where access to the on-chip bus is granted to requesting bus transactions

13 based at least in part on the included bus arbitration priorities of the contending bus

14 transactions.

1 13. The subsystem of claim 12, wherein the data transfer unit further comprises

2 a first and a second inbound queue to facilitate selective staging of a first and

3 a second plurality of inbound bus transactions for the core subsystem logic, at the

4 choosing of originating subsystems of the inbound bus transactions, each of the

5 inbound bus transaction including a bus arbitration priority and being granted access

6 to the on-chip bus based at least in part on the included bus arbitration priority; and

7 a second state machine coupled to the first and second inbound queues to

8 service the first and second inbound queues, serially bringing the staged inbound

9 bus transactions to the attention of the core subsystem logic, according the first

10 inbound queue a first inbound priority and the second inbound queue a second

11 inbound priority.

1 14. The subsystem of claim 13, wherein said data transfer block further

2 comprises a configuration register coupled to said second state machine to store

3 said first and second inbound priorities to be accorded to said first and second

4   inbound queues by said second state machine in servicing said first and second

5   inbound queues.

1   15.   The subsystem of claim 10, wherein

2   the data transfer block further comprises a third inbound queue, which in

3   conjunction with said first and second inbound queues, facilitates selective staging of

4   a third and said first and second plurality of inbound bus transactions for the core

5   subsystem logic, at the choosing of originating subsystems of the inbound bus

6   transactions, with each of the inbound bus transactions including a bus arbitration

7   priority, and granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   said second state machine is also coupled to said third inbound queue, and

10   service said third inbound queue, along with said first and second inbound queues,

11   serially bringing the staged inbound bus transactions to the attention of the core

12   subsystem logic, according the third queue a third inbound priority complementing

13   said first and second inbound priorities accorded to the first and second inbound

14   queues.

1   16.   The subsystem of claim 10, wherein the subsystem is a selected one of a

2   memory controller, a security engine, a voice processor, a collection of peripheral

3   device controllers, a framer processor, and a network media access controller.

1   17.   A subsystem of an integrated circuit, the subsystem comprising:

2   core subsystem logic; and

3   a data transfer unit to couple the core subsystem logic to an on-chip bus of

4   the integrated circuit, the data transfer unit including

5   a first and a second inbound queue to facilitate selective staging of a first

6   and a second plurality of inbound bus transactions for the core

7   subsystem logic, at the choosing of originating subsystems of the

8   inbound bus transactions, each of the inbound bus transaction

9   including a bus arbitration priority and being granted access to the on-

10   chip bus based at least in part on the included bus arbitration priority;

11   and

12   a state machine coupled to the first and second inbound queues to service

13   the first and second inbound queues, serially bringing the staged

14   inbound bus transactions to the attention of the core subsystem logic,

15   according the first inbound queue a first inbound priority and the

16   second inbound queue a second inbound priority.

1   18.   The subsystem of claim 17, wherein said data transfer unit further comprises

2   a configuration register coupled to said state machine to store said first and second

3   inbound priorities to be accorded to said first and second inbound queues by said

4   state machine in servicing said first and second inbound queues.

1   19.   The subsystem of claim 17, wherein

2   the data transfer block further comprises a third inbound queue, which in

3   conjunction with said first and second inbound queues, facilitates selective staging of

4   a third and said first and second plurality of inbound bus transactions for the core

5   subsystem logic, at the choosing of originating subsystems of the inbound bus

6   transactions, with each of the inbound bus transactions including a bus arbitration

7   priority, and granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   said state machine is also coupled to said third inbound queue, and service

10   said third inbound queue, along with said first and second inbound queues, serially

11   bringing the staged inbound bus transactions to the attention of the core subsystem

12   logic, according the third queue a third inbound priority complementing said first and

13   second inbound priorities accorded to the first and second inbound queues.

1   20.   The subsystem of claim 17, wherein the subsystem is a selected one of a

2   memory controller, a security engine, a voice processor, a collection of peripheral

3   device controllers, a framer processor, and a network media access controller.

1   21.   In a subsystem of an integrated circuit, a method of operation comprising:

2   determining intra-subsystem priorities for transactions with others subsystems

3   of the integrated circuit to be serviced for requesting access to an on-chip bus of the

4   integrated circuit, to which the subsystems are coupled;

5   generating and staging the transactions in accordance with the determined

6   intra-subsystem priorities, including with each of the staged transactions a bus

7   arbitration priority for use to arbitrate for access to the on-chip bus with other inter-

8   subsystem transactions of other subsystems of the integrated circuit; and

9   serially servicing the staged transactions in accordance with their intra-

10   subsystem priorities, requesting access to the on-chip bus for each staged

11   transaction being serviced using the included bus arbitration priority.

1   22.   The method of claim 21, wherein said generating and staging comprises

2   generating and staging each of the transactions in a selected one of a plurality of

3   outbound queues in accordance with the determined intra-subsystem priorities,

4   including with each of the staged transactions a bus arbitration priority for use to

5   arbitrate for access to the on-chip bus with other inter-subsystem transactions of

6   other subsystems of the integrated circuit.

1   23.   The method of claim 21, wherein the method further comprises

2   staging transactions from other subsystems in a priority based manner as

3   requested by originating subsystems of the transactions, each of said transactions

4   from other subsystems having a bus arbitration priority, on which access to a on-chip

5   bus was granted; and

6   serially servicing the staged transactions from other subsystems, notifying

7   core logic of the subsystem, in accordance with the priority based manner the

8   transactions from other subsystems are staged.

1   24.   The method of claim 23, wherein said staging of transactions from other

2   subsystems comprises staging each of the transactions from other subsystems in a

3   selected one of a plurality of prioritized inbound queues as requested by the

4   originating subsystems of the transactions.

1   25.   In a subsystem of an integrated circuit, a method of operation comprising:

2   staging transactions from other subsystems in a priority based manner as

3   requested by originating subsystems of the transactions, each of said transactions

4   from other subsystems having a bus arbitration priority, on which access to a on-chip

5   bus the subsystems are coupled was granted; and

6   serially servicing the staged transactions from other subsystems, notifying

7   core logic of the subsystem, in accordance with the priority based manner the

8   transactions from other subsystems are staged.

1   26.   The method of claim 25, wherein said staging of transactions from other

2   subsystems comprises staging each of the transactions from other subsystems in a

3   selected one of a plurality of prioritized inbound queues as requested by the

4   originating subsystems of the transactions.

1   27.   An integrated circuit comprising:

2   an on-chip bus; and

3   a plurality of subsystems coupled to the on-chip bus and interact with each

4 other through transactions conducted across said on-chip bus, with each of the

5 subsystems having a data transfer interface that interfaces the subsystem to the on-

6 chip bus, and at least one of the data transfer interfaces allows the particular

7 subsystem to initiate transactions with other subsystems in a prioritized manner,

8 including a first intra-subsystem prioritization on the order transactions contending

9 for the service of the at least one of the data transfer interfaces are to be serviced,

10 and a second inter-subsystem prioritization on the order transactions of the various

11 subsystems contending for the on-chip bus are to be granted access to the on-chip

12 bus.

1   28.   The integrated circuit of claim 27, wherein the at least one of the data transfer

2 interfaces comprises

3   a first and a second outbound queue to facilitate selective staging of a first

4 and a second plurality of outbound bus transactions for the particular subsystem, at

5 the choosing of core logic of the particular subsystem, with each of said outbound

6 bus transactions including a bus arbitration priority; and

7   a first state machine coupled to the first and second outbound queues to

8 service the first and second outbound queues, serially requesting for access to the

9   on-chip bus for the staged outbound bus transactions, according the first queue a

10 first outbound priority and the second queue a second outbound priority, where

11 access to the on-chip bus is granted to requesting bus transactions based at least in

12 part on the included bus arbitration priorities of the contending bus transactions.

1   29.   The integrated circuit of claim 28, wherein the at least one of the data transfer

2   interfaces further comprises

3   a first and a second inbound queue to facilitate selective staging of a first and

4   a second plurality of inbound bus transactions for core logic of the particular

5   subsystem, at the choosing of originating subsystems of the inbound bus

6   transactions, each of the inbound bus transaction including a bus arbitration priority

7   and being granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   a second state machine coupled to the first and second inbound queues to

10 service the first and second inbound queues, serially bringing the staged inbound

11 bus transactions to the attention of the core logic of the particular subsystem,

12 according the first inbound queue a first inbound priority and the second inbound

13 queue a second inbound priority.

1   30.   The integrated circuit of claim 27, wherein the at least one of the data transfer

2   interfaces comprises

3   a first and a second inbound queue to facilitate selective staging of a first and

4   a second plurality of inbound bus transactions for core logic of the particular

5   subsystem, at the choosing of originating subsystems of the inbound bus

6   transactions, each of the inbound bus transaction including a bus arbitration priority

7   and being granted access to the on-chip bus based at least in part on the included

8   bus arbitration priority; and

9   a state machine coupled to the first and second inbound queues to service

10   the first and second inbound queues, serially bringing the staged inbound bus

11   transactions to the attention of the core logic of the particular subsystem, according

12   the first inbound queue a first inbound priority and the second inbound queue a

13   second inbound priority.

1   31.   The integrated circuit of claim 27, wherein the subsystems are selected ones

2   of a memory controller, a security engine, a voice processor, a collection of

3   peripheral device controllers, a framer processor, and a network media access

4   controller.

1   32.   In an integrated circuit having an on-chip bus and a plurality of subsystems

2   coupled to each other via the on-chip bus, a method of operation comprising:

3   a first subsystem having a first data transfer interface interfacing the first

4   subsystem to the on-chip bus, initiating first transactions with other subsystems

5   through selective employment of facilities of the first data transfer interface to

6   internally prioritizing the order the first transactions are to be serviced by the first

7   data transfer interface, and including with said first transactions first bus arbitration

8   priorities to facilitate prioritization of granting of access to the on-chip bus to

9   contending inter-subsystem transactions including said first transactions; and

10   a second subsystem having a second data transfer interface interfacing the

11 second subsystem to the on-chip bus, initiating second transactions with other

12 subsystems through selective employment of facilities of the second data transfer

13 interface to internally prioritizing the order the second transactions are to be serviced

14 by the second data transfer interface, and including with said second transactions

15 second bus arbitration priorities to facilitate prioritization of granting of access to the

16 on-chip bus to contending inter-subsystem transactions including the second

17 transactions.

1   33.   The method of claim 32, wherein the method further comprises the first data

2   transfer interface of the first subsystem staging third transactions from other

3   subsystems in a priority based manner as requested by originating subsystems of

4   the third transactions, said third transactions from other subsystems also having

5   third bus arbitration priorities, based on which accesses to said on-chip bus were

6   granted;

1   34.   The method of claim 33, wherein the method further comprises the first data

2   transfer interface of the first subsystem serially servicing the staged third

3   transactions from other subsystems, notifying core logic of the first subsystem, in

4   accordance with the priority based manner the third transactions from other

5   subsystems are staged.

1   35.   The method of claim 33, wherein the method further comprises the second

2   data transfer interface of the second subsystem staging fourth transactions from

3   other subsystems in a priority based manner as requested by originating

4   subsystems of the fourth transactions, said fourth transactions from other

5   subsystems also having fourth bus arbitration priorities, based on which accesses to

6   said on-chip bus were granted.